Low Power, Low Group Delay MB-OFDM UWB CMOS Power Amplifier Using Current-Reused Technique

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Abstract—**This paper presents a low power and low group delay for multiband orthogonal frequency division multiplexing (MB-OFDM) ultra wideband (UWB) power amplifier (PA) for 3.1-7.5 GHz is proposed. The proposed PA employs a common gate with current-reused structure to provide wideband input matching, low group delay and low power consumption. The simulation results shows that the proposed PA design has an average gain of 11.4 dB with flatness of ±0.8 dB, while maintaining bandwidth of 2.6 to 8.3 GHz. An input return loss (S_{11}) less than -11.1 dB and output return loss (S_{22}) less than -10.5 dB, respectively are obtained. The PA design achieves the phase linearity (i.e. group delay) of ±67.1 ps and only consuming 14.5 mW power from 1.2 V supply voltage. A good output 1-dB compression point OP_{1dB} of 0.5 dBm is obtained.**

Keywords-power amplifier; common gate confguration; current-reused; group delay; low power; ultra-wideband (UWB).

I. INTRODUCTION

Ultra wide band technology has great growing demand and become more popular which is capable of transmitting higher data rate over a wide frequency for short range with low power. In 2002, the Federal Communication Commission (FCC) officially released the regulation for UWB technology with the allocated frequency band of 3.1-10.6 GHz. Two major solution under consideration for UWB transceiver are proposed, namely multiband orthogonal frequency division multiplexing (MB-OFDM) and direct-sequence code division multiple access (DS-CDMA) [1]. In MB-OFDM proposal, the frequency range from 3.1–10.6 GHz is divided in 14 channels into five groups with 528 MHz for each channel. Frequency band from 3.1 to 7.92 GHz is in Group 1, Group 2, and Group 3, respectively [2].

Until now, several UWB PAs have been reported for frequency of 3.0–5.0 GHz (Group 1) [3], 3.0–7.0 GHz (Group 1 to Group 3) [4], 6.0–10.0 GHz (Group 4 to Group 5) [5] and 3.1-10.6 GHz (Group 1 to Group 5) [6] with different kind of topologies such as distributed amplifier, RLC matching topology, resistive shunt feedback amplifier, and current-reused technique. The distributed amplifier provides wideband matching and linearity. However, it consumes more power, and uses a large area of chip [7]. The RLC matching also offers wideband matching but needs a large area of chip due to the number of reactive elements are used to form RLC filter [8]. The shunt feedback amplifier can provide flat gain and good wideband matching however, difficulty to achieve 50Ω input matching makes it impractical [9]. Most of reported UWB PAs have high power consumption and high group delay in the design. Even previous reported works have shown that increasing frequency bandwidth has tendency to deteriorate the group delay and power.

As UWB PAs are supposed to transmit the signal at short distance with very low power, it is a motivation to design UWB PA with low power consumption and low group delay which is used as criteria to evaluate phase nonlinearity. It is very important to keep a small group delay variation in frequency band because this implies that if the group delay varies to frequency, the time domain waveform becomes distorted especially for UWB system using impulse signal [10]. It means that output does not retain its original identity without a PA of smaller group delay. Therefore, the author had also proposed for 3.0-7.5 GHz using current reused technique to obtain low power consumption and very low group delay. To the best of our knowledge, the proposed UWB PA implemented in 0.18μm technology has obtained excellent group delay, low power,and average gain flatness so far compared to other works reported for UWB PAs.

II. UWB PA DESIGN

The proposed UWB PA is shown in Figure 1 which consists of two stages of amplifier. The first stage consists of current-reused structure where M_1 is common gate amplifier and M_2 is common source amplifier. Note that M_2 is also a common source amplifier converted from a common gate amplifier by current-reused technique. Common gate amplifier, M_1 is used to provide wideband input matching, good linearity, input-output isolation, but its parasitic capacitance of transistor will degrade the PA power gain performance in the high frequency region. Therefore, two stages of amplifier are employed to reach sufficient power gain, while maintaining a

wide bandwidth for entire frequency of interest. L_2 and C_2 of M_2 are employed to provide low impedance, while L_3 has adequately large impedance to provide high path to block the signal at frequency of interest. Under current-reused structured, the input signal can be amplified twice and the current gain becomes [11]:

$$i_{ds2} = \frac{g_{m2}}{sC_{gs2}} \times i_{ds1} \qquad (1)$$

$$\frac{i_{ds2}}{i_{ds1}} \approx \frac{\omega_T}{\omega} \qquad (2)$$

where ω_T is cut-off frequency of M_2 and ω is the operation frequency. The resonant circuit of L_2 and C_2 which perform narrowband characteristic are employed to enhance the gain at the upper end of the desired band i.e. 7.5 GHz. The shunt inductor L_4 inductively peaks at lower frequency (i.e. 3.1 GHz) which improves the gain at a low frequency. Hence, the wider bandwidth can be achieved. The second stage is a common source amplifier to enhance the gain. L_5 and R_4 are employed to have a peaking characteristic to widen the bandwidth as well as to improve the output return loss. C_2 is also added to improve broadband output impedance of 50Ω matching over the entire bandwidth. The entire shunt peaking load, L_4, L_5, R_2, and R_4 in the proposed PA are needed to compensate for bandwidth limitation and increase the gain flatness bandwidth of the output stage. Therefore, to achieve 60% bandwidth extension with an optimum group delay, which is desirable for optimizing pulse fidelity in a broadband system, the shunt peaking inductor L and resistor are designed [12]. A simple LC network of C_1 and L_1 is employed to achieve 50Ω input matching network. C_1 also serves as dc blocking and C_3 is the bypass capacitor.
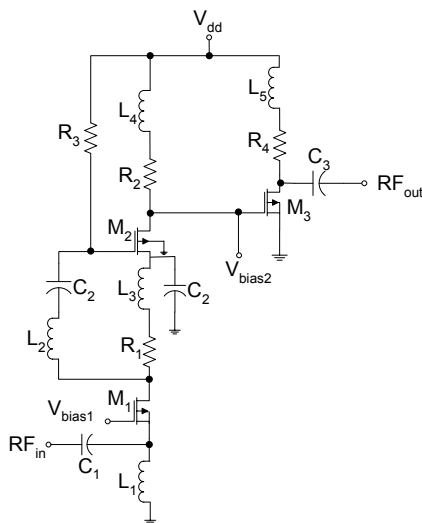

Figure 1: The proposed 3.1-7.5 GHz CMOS UWB PA

III. POST LAYOUT SIMULATION RESULTS

The post layout simulation of proposed PA is performed using Cadence SpectreRF simulator in 0.18μm CMOS process with 1.2V supply voltage. The input port and output port are matched with 50Ω resistance during simulation. The layout is shown in Figure 2 with size of 0.99 mm x 0.96 mm. This layout is already taped out for fabrication.

The simulated S-parameter is shown in Figure 3. As can be seen the simulated gain of the proposed PA has an average gain of 11.4 ± 0.8 dB from 3.1 to 7.5 GHz while maintaining a 3-dB bandwidth of 2.6 to 8.3 GHz. The input return loss (S_{11}) is less than -11.1 dB and the output return loss (S_{22}) is less than -10.5 dB. The proposed PA has achieved a good reverse isolation of 37 dB over frequency range of 3.1 to 7.5 GHz as illustrate in Figure 4. In addition, the minimum stability K-factor of this amplifier of more than 10 is achieved from 3.1-7.5 GHz as shown in Figure 5. The total power consumption of the proposed PA is only 14.5 mW. As illustrate in Figure 6, it can be seen that excellent phase linearity (i.e. group delay) of ±67.1 ps is obtained. Further improvement in the group delay can be done by improving the input matching and output matching. The simulated input 1-dB compression point (IP1dB) and output 1-dB compression point (OP1dB) is depicted in Figure 7. The IP1dB is -9.8 dBm and OP1dB is 0.5 dBm at 5 GHz.

Table 1 summarizes the performance of recently published UWB PAs. As can be seen that the proposed UWB PA has obtained average gain flatness, excellent group delay, and has the lowest low power so far compared to other works reported on the full band UWB PAs. With these characteristics the proposed is suitable for Group 1-3 of MB-OFDM UWB transmitter.
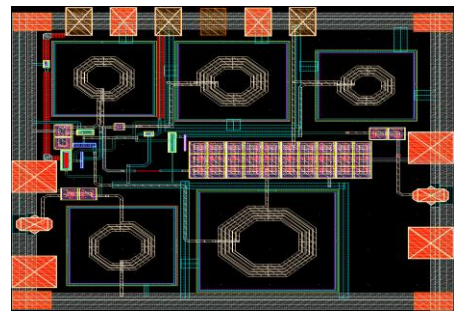

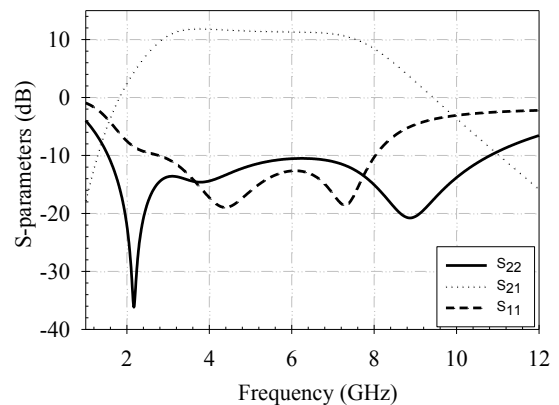Figure 2: Chip micrograph of the proposed PA (0.99 x 0.968mm)
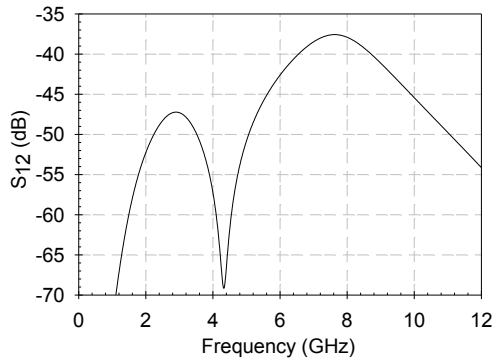

Figure 3: Simulated S-parameters

Figure 4: Simulated reverse isolation

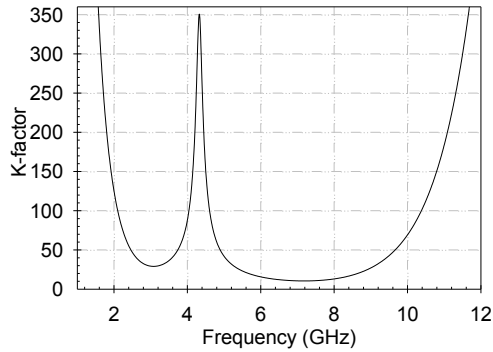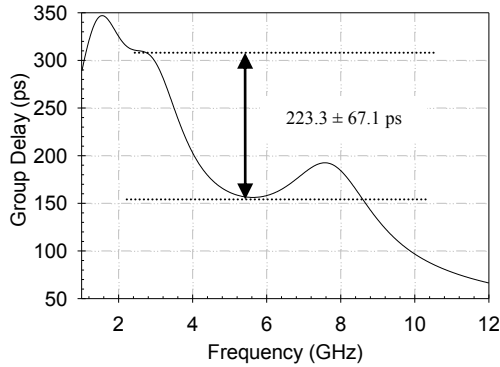Figure 5: Simulated K-factor

Figure 6: Simulated group delay versus frequency
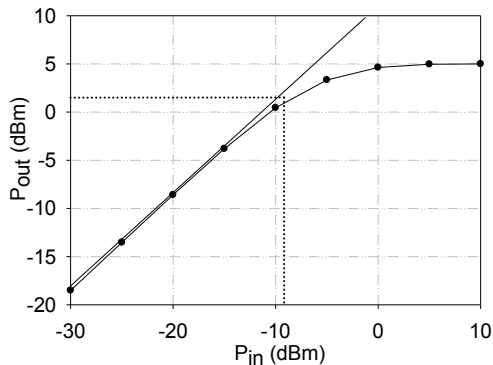
223.3 ± 67.1 ps

Figure 7: Simulated IP1dB and OP1dB

Table 1: Comparison of Wideband CMOS PA Performances: Published and Present Works

Ref	[3]	[4]	[5]	[6]	[13]	This work
CMOS technology (µm)	0.18	0.18	0.18	0.18	0.18	0.18
Frequency (GHz)	3.1-5.0	3.0-7.0	6.0-10	3.0-10	3.7-8.8	3.1-7.5
Vdd(V)	1.8	1.8	1.5	2.0	N/A	1.2
OP_{1dB}(dBm)	-3.4	7.0	5.0	5.6	15.6	0.5
Gain (dB)	15.2 ±0.6	14.5 ± 0.5	8.5	10.4 ±0.8	7.15 ±1.2	11.4 ±0.8
S_{11} (dB)	<-5	<-6	<-7	<-10	N/A	<-11.1
S_{22} (dB)	<-6	<-7	<-7	<-10	<-8	<-10.5
Power (mW)	25	24	18	84	154	14.5
GD (ps)	N/A	±178.5	N/A	±250	N/A	±67.1
Area (mm^2)	1.65	0.88	1.08	1.76	2.8	0.95

IV.   CONCLUSION

In this paper, a low power and low group delay has been design using 0.18µm CMOS technology. The proposed amplifier adopts common gate with current-reused technique to provide good input matching, low group delay, low power and linearity. The simulation results show that the proposed design PA offers an average gain of 11.4 dB with flatness of ±0.8 dB while maintain a 3-dB bandwidth of 2.6 to 8.3 GHz. An input return loss (S_{11}) and output return loss (S_{22}) less than -11.1 dB and -10.5 dB, respectively were obtained. The PA design achieves the phase linearity of ±67.1 ps, and consumes only 14.5mWpower from 1.2 V supply voltage. A good input 1dB compression and output 1dB point are -9.8 dBm and 0.5 dBm, respectively at 5 GHz.

REFERENCES

[1] WPAN High Rate Alternative PHY Task Group 3a (TG3a), IEEE 802.15, 2007 [online].
Available: http://www.ieee802.org/15/pub/TG3a.html

[2] W.-C. Wang, C-P. Liao, Y.-K. Lo, Z.-D. Huang F. R. Shahroury, and C.-Y. Wu, "The design of integrated 3-GHz to 11-GHz CMOS transmitter for fullband ultra-wideband (UWB) applications," *in IEEE International Symposium on Journal of Circuits and Systems*, May 18-21, 2008, pp. 2709-2712.

[3] S.K. Wong, S. Maisurah, M.N. Osman, F. Kung and J.H. See, "High efficiency CMOS power amplifier for 3 to 5 GHz Ultra-Wideband (UWB) Application," *IEEE Transaction on Consumer Electronics*, vol.55, No.3, August 2009, pp. 1546-1550.

[4] S.Z Murad, R.K Pokharel, A. Galal, R. Sapawi, H. Kanaya and K. Yoshida, "An Excellent Gain Flatness 3.0-7.0 GHz CMOS PA for UWB Applications", *IEEE Microwave and Wireless Component Letters,* vol.20, no 9, September 2010.

[5] H-W Chung, C-Y. Hsu, C-Y. Yang, K-F. Wei, H-R. Chuang, "A 6-10 GHz CMOS power amplifier with an inter-stage wideband impedance transformer for UWB transmitters," *in proc 38th European Microwave Conference*, pp. 305-308, 27-31 Oct. 2008.

[6] C. Lu, A-V. Pham, and M. Shaw, "A CMOS power amplifier for full-band UWB transmitters", *in Proc. IEEE Radio Frequency Integrated Circuit (RFIC) Symposium 2006*, pp.400, 11-13 June 2006.

[7] C. Grewing, K. Winterberg, S.V Waasen, M. Friedrich, G.L Puma, A. Wiesbaure and C. Sandner, "Fully integrated distributed power amplifier in CMOS technology, optimized for UWB transmitter," *IEEE RF IC Symposium*, August 2004

[8] H.C. Hsu, Z.W. Wang and G. K. Ma, "A low power CMOS full-band UWB power amplifier using wideband RLC matching method," *IEEE Conference on Electron Devices and Solid-State Circuit*, pp. 233-236, 19-21 December 2005.

[9] S. Jose, H.J Lee and D. Ha, "A low power CMOS PA for UWB applications," *IEEE Int. Symposium on Circuits & Systems, ISCAS 2005*, vol. 5, pp. 5111-5114, 23-26 May 2005.

[10] K.Murase, R. Ishikawa and K. Honjo, "Group delay equalized monolithic microwave integrated circuit amplifier for ultra-wideband based on right/ left-handed transmission line design approach," *IET Microwave, Antenna & Propagation*, vol. 3, pp. 967-973, 2009.

[11] H.L. Kao and K.C. Chang, "Very low-power CMOS LNA for UWB wireless receivers using current-reused topology," Solid-State Electronics, vol.52, issue 1, pp. 86-90, Jan. 2008.

[12] S. Mohan, M. Hershenson, S. Boyd and T. Lee, "Bandwidth extension in CMOS with optimized on-chip inductor," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346-355, March 2005.

[13] C. Lu, A-V. Pham , M. Shaw, and C. Saint, "Linearization of CMOS broadband power amplifier through combined multigated transistors and capacitance compensation," *IEEE Trans. Microwave Theory Tech.*, vol.55, no. 11, pp. 2320-2328, November 2007.